Wen Tian

(+1) 8583618819 | went@andrew.cmu.edu | https://wen-tian-pineapple.github.io/

"Be the change that you want to see in the world."

Summary

Incoming ECE Phd @CMU, have experience in industry and academia related to hardware / software system

Education

University of Michigan Ann Arbor
UofM, USA

Master in Electrical Engineering — *Aug. 2022 - May. 2024*

- GPA 3.927
- VLSI track

University of California San Diego
UCSD, USA

Bachelor of Science in Computer Engineering — *Sep. 2020 - Jun. 2022*

- GPA 3.917(Major GPA 4.0)
- Warren College Honors community

Stony Brook University, New York
SBU, USA

Bachelor of Science in Computer Engineering and Computer Science — *July. 2018 - Aug. 2020*

- GPA 4.0
- honor college community

Research Experience

VLSI CAD Lab & WCSNG Lab
San Diego, USA

University of California San Diego — *Jan. 2021 - Aug. 2022*

- OpenRoad Project
  - Improve HPWL(half perimeter wire length) calculator to reduce wire length.
  - Improve cell placement to reduce pin congestion.
- Back Scattering Project
  - Design and implement the testing platform for back scattering BTLE signal.([ISSCC 2022])

Michigan Integrated Circuit Lab (MICL)
Ann Arnor, USA

University of Michigan Ann Arbor — *Feb. 2023 - June. 2024*

- OpenFASOC Project
  - Implement a special router feature that routes the power nets to standard cells.
  - Implement a Reinforcement Learning capability with new AMS automation tool in OpenFASOC.([ICCAD 2024] & [ISSCC 2024 code-a-chip competition]
- GPGPU simulator Project
  - Conduct performance analysis of Nvidia confidential computing architecture with large language model like lama.

EIC Lab
Georgia, USA

Georgia Institute of Technology — *July. 2024 - Feb. 2025*

- Freely Interruptible Progressive Large Model Inference Project
  - Design hardware architecture/micro-architecture and Dataflow.

Work Experience

RiVAI Technologies
Shenzhen, Guangdong, China

RTL Design Engineer
Nov. 2024 - now

- NoC & System Group
  - Micro-architecture and RTL design and implementation for RAS/DEBUG/Die2Die bridge modules.

DHC software
Nanchang, JiangXi, China

Software Develop Engineer
Jun. 2020 - Jun. 2021

- Design software interface and web page.
- Use mimics20.0, 3-matic to create organ model.

Selected Course Project

Energy-efficient Sparsity-Aware CNN Accelerator(Taped out*)

EECS 627

- In this project, we present an energy-efficient and configurable deep convolutional neural network (CNN) accelerator supporting current CNNs, which can have many layers. The accelerator incorporates a array of multiple PEs including MAC and accumulator, a novel hardware called “scanner” to adjust input data, and a global buffer for data storage. The design uses a sparsity-aware strategy to reduce the processing time and energy consumption. The data movement and data reuse methods in this design enables it to achieve power saving requirements.

R10K out-of-order processor with N-way superscalar

EECS 470

- In this project, we design a R10K out-of-order processor with N-way superscalar implemented with Tomasulo’s algorithm with non-blocking instruction cache (Icache) with prefetching enabled, decoder, G-share branch predictor, return address stack (RAS), reservation stations (RS), reorder buffer (ROB), register alias table (RAT), retirement register alias table (RRAT), physical register file (PRF), function units (FU), seperated load-store queue (LSQ) with store to load forwarding and load to store forwarding, and non-blocking data cache (Dcache).

SRAM Array plus Multi-Logic Operations for Programmable In-Memory Vector Computing

EECS 427

- The overall architecture of this design mainly contains 5 parts, 128×64 SRAM bitcell array, controller, column driver, near-memory computing units, and interface with datapath. Once the calculation is done, the results are written back to the destination bitcell arrays, and the cycle ends. This SRAM array is capable of performing vector-based, bit-serial in-memory arithmetic operations such as integer addition, subtraction, and multiplication, enhancing the processing capabilities of a baseline processor up to an operation frequency of 300 MHz.

Skills

Computer architecture	Out-of-Order RISCV CPU
Programming	C/C++, Python, JAVA, LaTeX, bash, makefile, verilog, system verilog
Digital & Physical Design	Synopsys DC/Verdi/PrimeTime, Cadence Innovus

Publication

- Ali Hammoud & Wen Tian, Anhang Li, Ayushman Tripathi, Karthik Lakshmanan, Harsh Khandeparkar, Ryan Wans, Boris Murmann, Dennis Sylvester, Mehdi Saligane, *”Reinforcement Learning-Enhanced Cloud-Based Open Source Analog Circuit Generator for Standard and Cryogenic Temperatures in 130-nm and 180-nm OpenPDKs”*, 2024 ACM/IEEE International Conference on Computer-Aided Design (ICCAD).

Honors & Certification

2024	**IEEE SSCS “Code-a-Chip” Travel Grant Awards 2024**, IEEE	*Ann Arbor, U.S.A*
2022-2023	**Dean’s List**, UofM	*Ann Arbor, U.S.A*
2021	**Jetson AI Specialist certificate**, Nvidia	*San diego, U.S.A*
2021	**CLAD certification**, National Instrument	*San diego, U.S.A*
2020-2022	**Provost honor**, UCSD	*San diego, U.S.A*
2018-2020	**Dean’s List**, Stony Brook University	*New York, U.S.A*